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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,619	CAI ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,19,21-23 and 25-30* is/are rejected.

7)☒ Claim(s) *13,15-18,20 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because of following informalities.

On page 29, line 8, "performed" should read, "performance".

On page 3, paragraph [0007], "processor of FIG. 2" should read "processor of FIG. 1".

On page 6, paragraph [0020], line 4, "memory 110" should be "memory 140".

On page 6, paragraph [0021], line 7, "external unit" should be "external bus unit".

On page 10, paragraph [0031], equation (1) is missing.

On page 11, paragraph [0032], equation (2) is missing.

Appropriate corrections are required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1,4,6,9,11,21,22 are rejected under 35 U.S.C. 102(e) as being anticipated by Bearden et al. (US 2004/0205298 A1) herein after Bearden.

As per claims 1,6 and 21, Bearden teaches a method comprising:

Identify a prefetch depth; (paragraph [0108], base prefetch depth);

performing prefetching according to the identified prefetch depth; and

adjusting the performing prefetching as changes in the prefetch depth are detected. ([paragraph [0042], taught as read cache prefetch depth is adapted to increase or decrease in response to variations in the operational parameters).

As per claim 4 and 9, the reading of the data line from memory is inherent feature of the processor after adjusting the prefetch depth.

As per claim 11, Bearden teaches the operational parameter generator (fig 4, item 404), which keeps track of operational parameters such as disk latency (paragraph [0061]) and updates the performance metrics and performance metrics is used to adjust the prefetch depth (paragraph [0067]).

As per claims 14,19 and 22 Bearden teaches the operational parameter generator looks up a disk drive latency, cache capacity to adjust the prefetch depth (paragraph [0061], lines 4-8, and paragraph [0067], lines 7-10) and hence teaches the tracking of memory subsystem response level (paragraph [0062]) and requests and occupancy level.

As per claim 25, Bearden teaches tracking of disk drive latency and cache capacity and workload parameters (paragraph [0061]) and inherently teaches memory occupancy detection logic and memory subsystem response level (paragraph [0040] teaches prefetch depth adapter is configured to execute on the processor).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-3,5, 7-8,10,12,23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bearden et at. (US 2004/0205298 A1) as applied to claim 1 above, and further in view of Schulz (US 2004/0148470 A1).

As per claims 2 and 7, Bearden teaches the parameter metrics and the prefetch adapter maps the value representing an amount of data that will be prefetched. (paragraph [0042], lines 9-14) and hence teaches a data structure. Bearden fails to teach if prefetching is enabled or not. Schulz teaches checking if prefetching is enabled or not via an enable signal. (fig 4, block 440, paragraph [0057]). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the prefetching method of Bearden by allowing enabling or disabling of the prefetching as taught by Schultz. As taught by applicant's admitted prior art aggressive prefetching drives up the memory subsystem usage and performance drops below non-prefetching levels (specification, page 2, lines 5-9). So disabling prefetching in some cases improves the system performance.

As per claims 3 and 8, Bearden teaches metrics that the prefetch depth adapter (fig. 2, item 234) generates the performance parameters and adjusts the prefetching depth according to the metrics (paragraph [0042]) and hence teaches accessing a table

entry and reading of table entry as the identified prefecth depth (as taught by prefetch depth value). The valid bit is just a method of checking whether prefetching is enabled or not (specification, page 10, paragraph [0030], if no entry is valid, CPU will not perform prefetching and page 14, paragraph [0043], the terms set, enable, assert includes assertion of signal indicating setting a bit value), which is taught by Schulz as in claim 2.

As per claims 5,10, 12 and 23 Bearden teaches that the prefetch depth adapter (fig 4, item 402) with operational parameter (fig. 4, item 404) and operational performance metric generator (fig. 4, item 406), which analyzes the performance parameters such as disk drive latency, cache capacity, workload etc. and creates a parametric table. The parametric table is adjusted according to those parameters (paragraph [0061]) and based on these metrics the prefetching depth is adjusted (paragraphs [0042] and [0067]). So Bearden teaches identification of update to prefetch data structure, and adjust the prefetching according to updated data structure. Identifying of the valid bit is just an indication of either the prefetching is enabled or not as taught in claims 3 and 8 above.

Claims 26-30 are rejected for the same rationale as applied to claims 1-10 above as Bearden teaches a system with controller, processor and I/O controller (figure 2, paragraphs [0030, 0031 and 0032])

Allowable Subject Matter

6. Claims 13,15-18,20 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin L. Ellis
Primary Examiner

Kaushikkumar Patel
Examiner
Art Unit 2188

KMP